REMARKS/ARGUMENTS

The Applicants respectfully request reconsideration of this Application. The Applicants originally submitted Claims 1-15 in the Application. The Applicants have previously amended Claims 1-8 and 10-14 and have canceled Claims 9 and 15. The Applicants again amend Claims 1 and 10, in accordance with the Examiner's suggestion. No claims have been added. Accordingly, Claims 1-8 and 10-14 are currently pending in the Application.

I. Rejection of Claims 1, 2, 4-8, 10-12 and 14 under 35 U.S.C. §102

The Examiner has rejected Claims 1, 2, 4-8, 10-12 and 14 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,201,308 to Ikegami. The teachings and deficiencies of Ikegami have been discussed in the prior Amendment and will not be repeated here. Independent Claims 1 and 10 have been amended in accordance with the Examiner's suggestion, to more clearly recite the structure of the claimed invention.

In contrast to the claimed invention, Ikegami does not disclose an electrically isolated trace formed at an outer region of a substrate that is free of electrical interconnection with components forming the integrated circuit disclosed therein. Rather, the traces disclosed in Ikegami are electrically interconnected with components therein to form an integrated circuit device, and thus, are not electrically isolated from each. As a result, the traces in Ikegami are not for testing the strength of the traces, as recited by the claimed invention. As a result, Ikegami does not anticipate the invention of Claim 1. Since independent Claim 10, as amended, recites elements analogous to those of Claim 1, Ikegami also does not disclose all the elements recited in Claim 10.

In conclusion, Ikegami does not teach the inventions recited in independent Claims 1 and 10 and, as such, is not an anticipating reference of these claims. In addition, dependent Claims 2,

4-8, 11-12 and 14 depend from Claims 1 and 10, respectively. Thus, Ikegami is also not an anticipating reference for these dependent claims. Accordingly, the Applicants respectfully request the Examiner withdraw the §102 rejection with respect to Claims 1, 2, 4-8, 10-12 and 14.

II. Rejection of Claims 3 and 13 under 35 U.S.C. §103

The Examiner has rejected dependent Claims 3 and 13 under 35 U.S.C. §103(a) as being unpatentable over Ikegami, as applied above, in view of U.S. Patent No. 5,811,874 to Lee. The Applicants respectfully assert that the claimed invention is nonobvious in view of the combination of the foregoing references, and that the combination does not established a *prima facie* case of obviousness of dependent Claims 3 and 13.

As discussed above, Ikegami does not teach an integrated circuit having a substrate with an electrically isolated trace that is free of electrical interconnection with components forming the integrated circuit, as recited in independent Claims 1 and 10. In addition, Ikegami does not suggest the use of such an electrically isolated trace, since the conductive traces disclosed in Ikegami are not used for testing the integrity of internal circuitry, but rather are electrically interconnected to help form an integrated circuit. In addition, Lee merely provides for chamferred regions along conductive traces to reduce the shear stress of the traces, and it does not teach or suggest the use of those conductive traces as electrically isolated test traces, but rather as part of the overall semiconductor chip device described therein. Therefore, since the combined teachings of Ikegami and Lee fail to teach or suggest all the inventions of independent Claims 1 and 10, the combination does not establish a *prima facie* case of obviousness of dependent Claims 3 and 13, which include the elements of independent Claims 1 and 10, respectively. Accordingly, a *prima facie* case of

obvious of Claims 3 and 13 has not been established, and the Applicants respectfully request the Examiner withdraw the §103 rejection of dependent Claims 3 and 13.

III. Conclusion

The Applicants respectfully request that the rejections be withdrawn and solicit a Notice of Allowance for Claims 1-8 and 10-14. The Applicants further attach hereto a marked-up version of the amendments made to the specification and the claims. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

Respectfully submitted,

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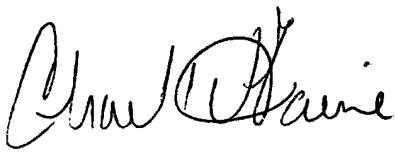

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

(1) Claim 1 has been amended as follows:

1. (Twice amended) An integrated circuit comprising:

a substrate;

a plurality of bond pads formed above the substrate; and

a first electrically isolated conductive trace formed at an outer region of the substrate and coupled to at least two of the plurality of bond pads.

(2) Claim 10 has been amended as follows:

10. (Twice amended) An integrated circuit comprising:

a substrate;

a plurality of bond pads; and

an electrically isolated conductive tester runner formed on the substrate and around the plurality of bond pads, the isolated conductive tester runner electrically coupled to at least two of the plurality of bond pads.